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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/675,336	09/29/2003	Yoo-Cheol Shin	4591-330	5312

20575 7590 08/01/2005

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EXAMINER	
HU, SHOUXIANG	
ART UNIT	**PAPER NUMBER**
2811	

DATE MAILED: 08/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/675,336	SHIN, YOO-CHEOL	
	Examiner	Art Unit	
	Shouxiang Hu	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 June 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *4-20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 June 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Claims 4-20 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim. Election was made **without** traverse in Paper No. 20041012.

Claim Objections

2. Claims 1-3 are objected to because of the following informalities and/or defects:

In claim 1, the term of "disposed on sidewalls" should read as: --disposed on one of two sidewalls--; otherwise the term of "resistor spacer" should be changed to : --spacers--

Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claim 1-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art ("AAPA") in view of Chang (Chang et al.; 6,004,841).

AAPA discloses a semiconductor device (Figs. 1-6 in the instant disclosure), comprising: a device isolation layer (42) disposed in a substrate (40) to define an active region; source and drain regions (40s and 40d) formed in the active region; a gate electrode (59) formed on the active region between the source and drain regions; a gate insulation layer (under the gate 59) interposed between the gate electrode and the active region; a resistor pattern (56b) formed on the device isolation layer (42); and resistor electrodes (58) connected to both ends of the resistor pattern, respectively, wherein the gate electrode includes a polysilicon layer (50) and a silicide layer (54) that are sequentially stacked on the gate insulation layer, and wherein the resistor pattern includes a single polysilicon layer (56b).

Although AAPA does not expressly disclose that the resistor pattern formed of a polysilicon layer can have spacer that protrudes above the pattern, one of ordinary skill in the art would readily recognize that such a spacer can be desirably formed on each sidewall of a polysilicon pattern for better protection of the edges of the pattern, as evidenced in the prior art of Chang (see the polysilicon pattern 8 and its spacers 10 in the cover page figure).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the spacer of Chang into to the device of AAPA, so that a semiconductor device with its resistor patterns being better protected would be obtained.

Regarding claim 2, it is noted that ONO layer (laminated silicon oxide/silicn nitride/silicon oxide) is art known multiple-layered gate insulation layer with high quality

dielectric characteristics, as readily evidenced in the prior art such as Kwon et al. (US 5,852,311; see the ONO layer 58 in the cover page figure).

Regarding claim 3, AAPA further teaches that the to form a semiconductor device shown in Fig. 1, comprising: a device isolation layer (12) disposed in a substrate (10) to define an active region; source and drain regions (30s and 30d) formed in the active region; a gate electrode (20a and/or 22) formed on the active region between the source and drain regions; a gate insulation layer (28 or the one under the gate layer 20a) interposed between the gate electrode and the active region; a resistor pattern (20b) formed on and in direct contact with the device isolation layer (12); and resistor electrodes (28) connected to both ends of the resistor pattern, respectively, wherein the resistor pattern includes a single polysilicon layer (56b).

Although AAPA does not expressly disclose that the gate layer 22 and the layer overlying it in the device shown in Fig. 1 can be formed of a polycide layer including a polysilicon layer underlying a silicide layer, one of ordinary skill in the art would readily recognize that such a polycide layer is desirably used to form the gate electrode for lowering the gate resistance, as readily evidenced in the prior art, including AAPA (see the first paragraph in the Background of the Invention section; also see the polycide gate layer (50 and 54) in Fig. 2).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to make the semiconductor device collectively taught above with the gate layer therein being made of a polycide layer, per the further

teachings AAPA, so that a semiconductor device with reduced gate resistance would be obtained.

Response to Arguments

5. Applicant's arguments with respect to claims 1-3 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shouxiang Hu whose telephone number is 571-272-1654. The examiner can normally be reached on Monday through Thursday, 7:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SH
July 27, 2005

SHOUXIANG HU
PRIMARY EXAMINER